

EinsyRetro 1.0b UltiMachine 11/08/2017

0.3a Revision Summary (for detailed information goto: <https://github.com/ultimachine/Einsy-Rambo/tree/0.3a>)

- Added TVS and over-voltage protection to select nets
- Added and corrected testpoints
- Added "XTRA0" net between 32U2 and 2560
- Removed via tenting underneath QFNs and other flat solder lug/heatsink primitives
- Added teardrops to vias
- Standardized via sizes to 10/22 and 15/30 (mils)
- New footprint for 5V SMPS inductor (fits two inductors now)
- Added I2C pullup footprints (resistors are "DNI")
- Fan connectors now have a 3rd pin for reading the TACH signal
- Added 100R to the gate of each FET
- Adjusted the stackup to better reflect a standard 4-layer stack

0.4a Revision Summary

- Touchup diode polarity markings in silkscreen
- New footprint for P3
- Moved thermistor TPs to connector pin
- Increased GND stitching
- Increased copper pour coverage
- Updated paste mask apertures on QFNs
- Added nAC_FAULT to pin_6 of Atmega2560
- Added J7, power failure relay input.
- Added R73
- Removed RN4
- Stole RX1 and TX1 from P1, moved to J19
- Combined 2560 ICSP (X18) with pins_9-14 of J19
- Removed J16-J18, X_MAX, Y_MAX, Z_MAX
- Changed X_MIN and Y_MIN endstops to 2-pin headers
- Changed Z_MIN endstop to Z_PROBE, 4-pin header
- Combined DIAG_0 and DIAG_1 on TMC2130 drivers
- TP40 moved 0.1" to the left
- TP32 moved 0.1" to the left

0.5a Revision Summary

- Added ferrites to motor controller outputs.
- Removed fuse and input filter for VMOT
- Move MOSFET pulldown resistors to input side of AND gates
- Added ferrites to all P1 and P2 signals.
- Changed RN1 and RN2 from 10k to 5.6k (increases voltage on motor controller Vref pins)
- Changed motor controller low-side I-sense resistors from 0.1 to 0.22Ohm
- Voltage regulator U3 is now sourced from VMOT (was +12V2)
- Added power bypass capacitors to J7 and J15
- +12V2(Logic) and +12V3(Bed) now have micro-controller ADC based voltage monitoring.
- Added 2 internal layers (now 6 layers total)
- Added filtered internal island for micro-controller Vcc
- Most bottom layer routing (Layer 6) was moved to the new adjacent internal layer (Layer 5)
- Moved MOSFET pulldowns R43 and R57 upstream from FETs and placed at input of AND gate.
- New pinout for J19 header.
- Motor connectors are now flush with the bottom edge of the board.

1.0a Revision Summary

- Populate FGND to GND resistor ties
- Changed motor drive sense resistors from 0.22R to 0.12R
- Added a 5V buck controller for more current and future flexibility
- Fan power is derived from 12V2 rail
- Hardware SPI nSS signal moved back to P2
- UART1 TX and RX moved back to P1

1.0b Revision Summary

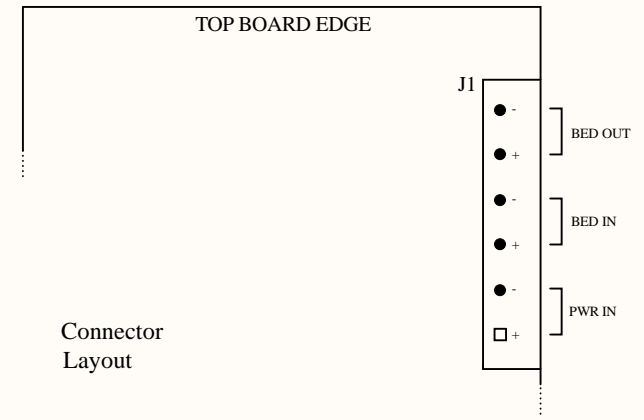
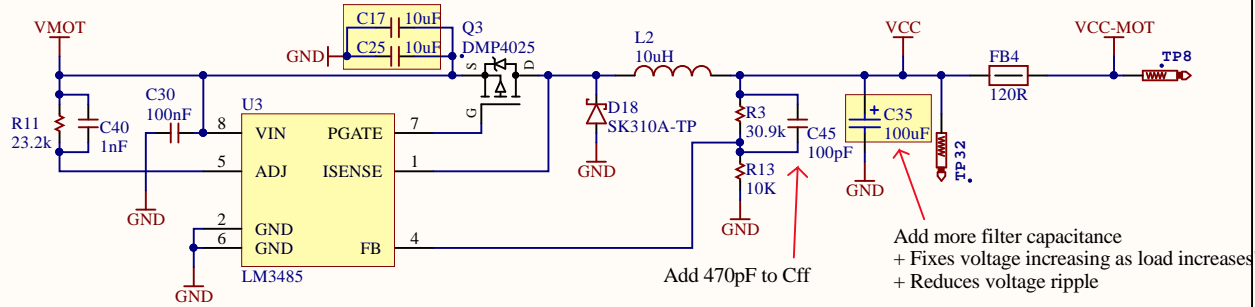
- Added 3-state buffer between SD_MISO_3V3 and MISO_5V0

Notes:

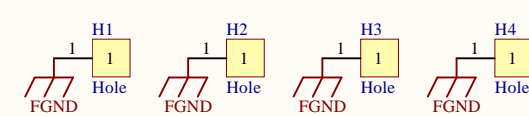
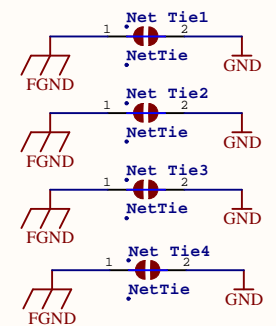
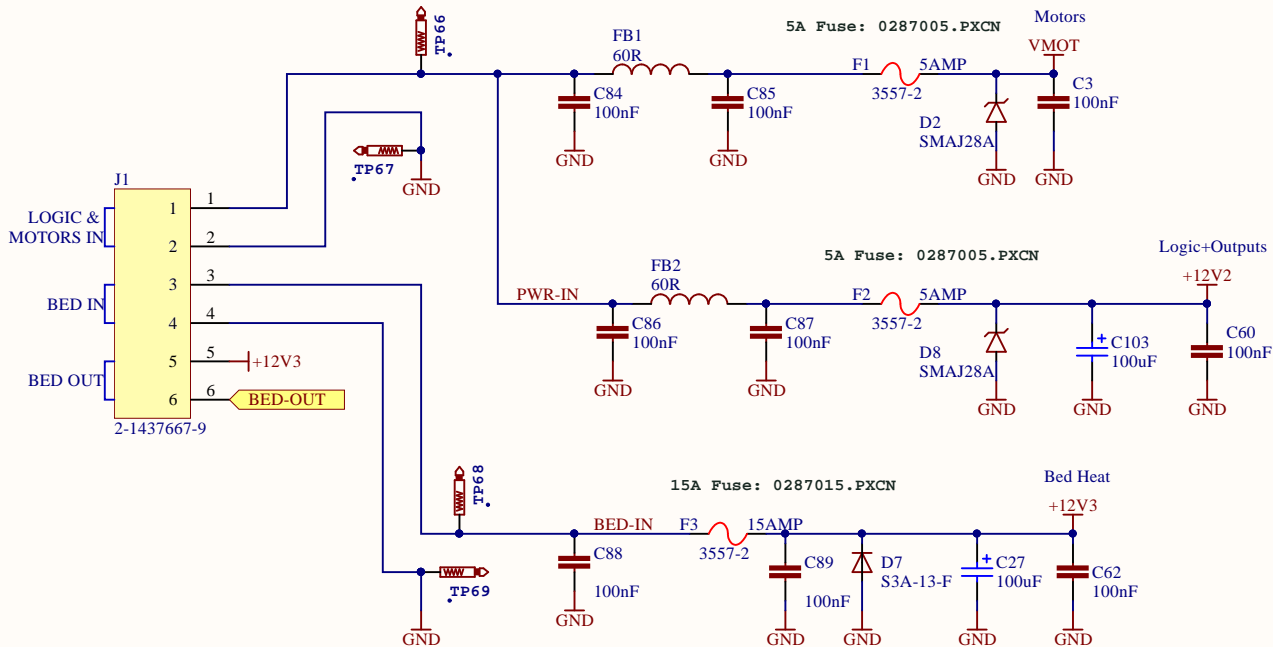
DNI = Do Not Include = No Populate

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Title: Title Page	File: Title.SchDoc
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Voltage Regulator

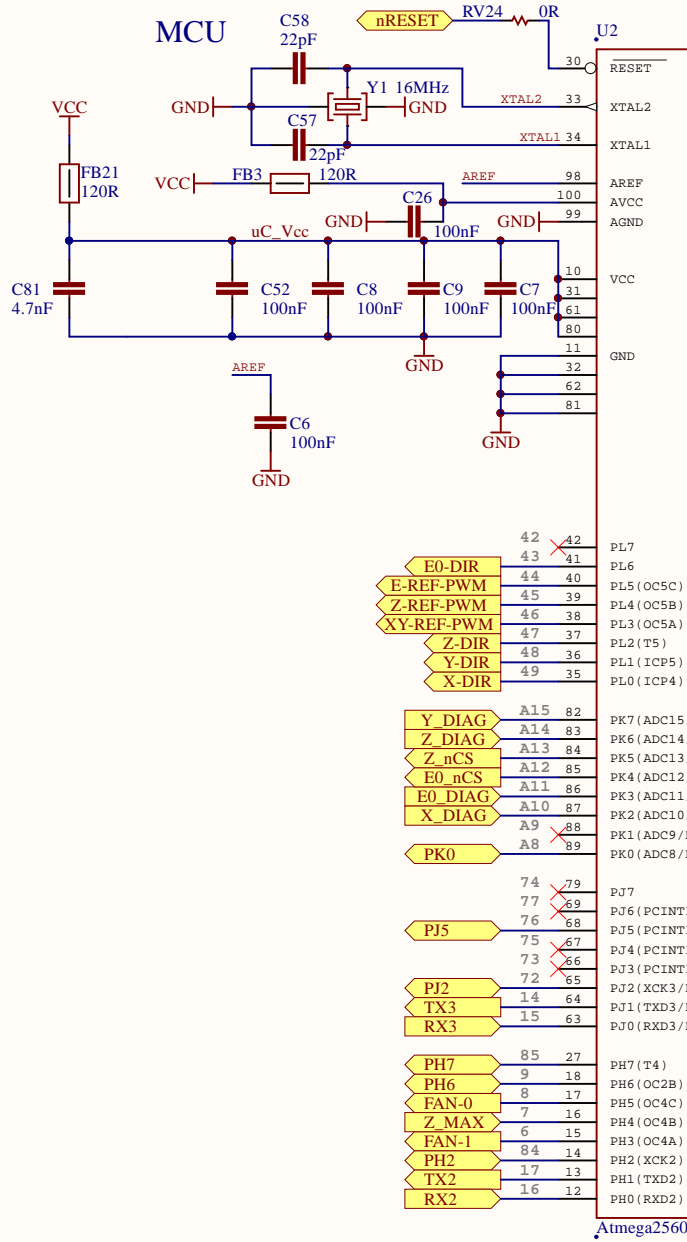


Power Input



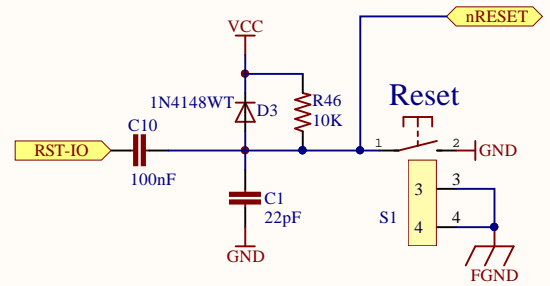
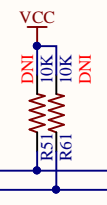
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Title: Power-SMPS	File: Power-SMPS.SchDoc
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MCU



Atmega2560

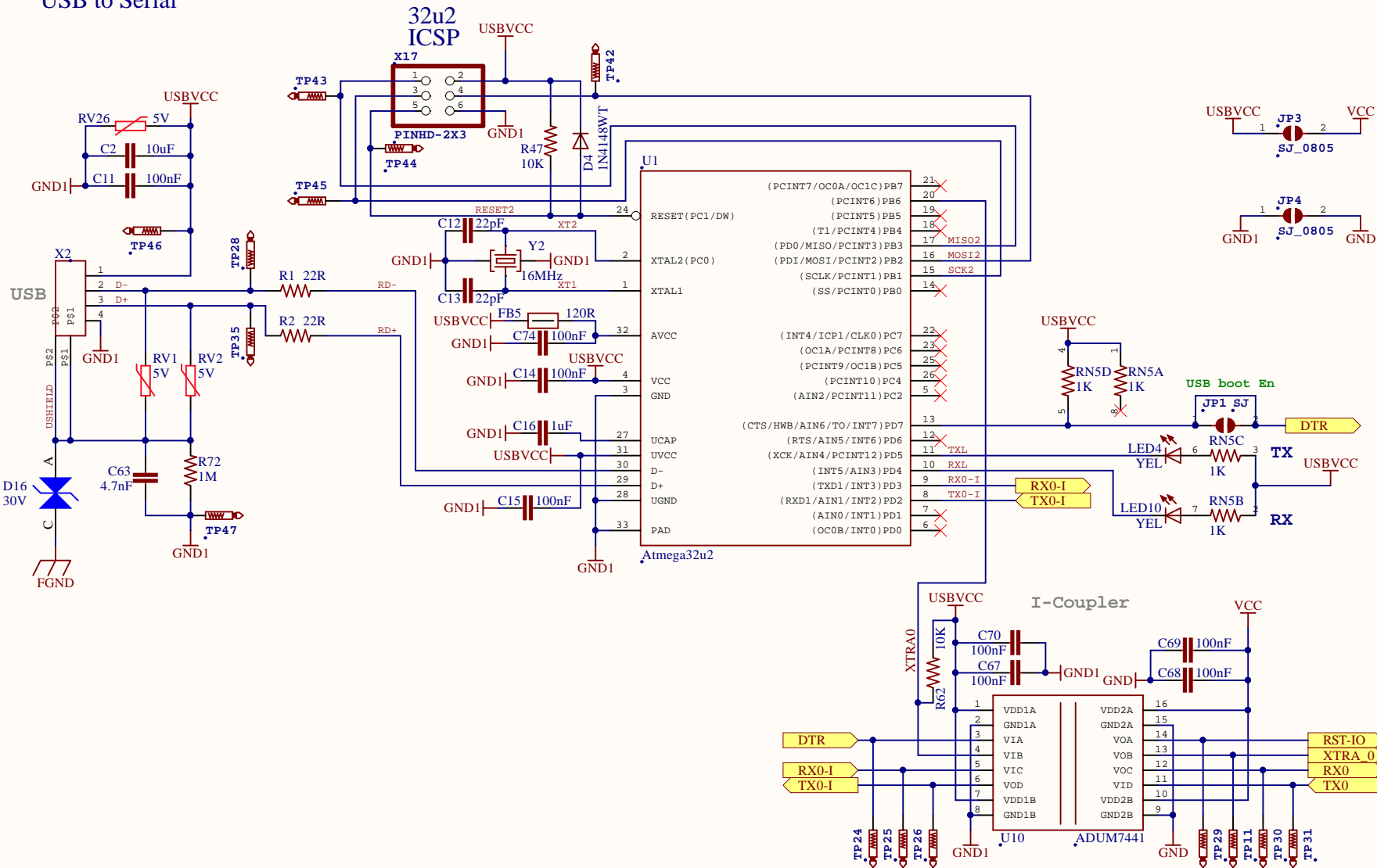
Part	Pin#	Arduino	Pin#
(AD7) PA7	71	29	X-EN
(AD6) PA6	72	28	Y-EN
(AD5) PA5	73	27	Z-EN
(AD4) PA4	74	26	E0-EN
(AD3) PA3	75	25	
(AD2) PA2	76	24	
(AD1) PA1	77	23	
(AD0) PA0	78	22	
(OC0A/OC1C/PCINT7) PB7	26	pwm 13	
(OC1B/PCINT6) PB6	25	pwm 12	
(OC1A/PCINT5) PB5	24	pwm 11	
(OC2A/PCINT4) PB4	23	pwm 10	
(MISO/PCINT3) PB3	22	50	
(MOSI/PCINT2) PB2	21	51	R27 22R RV8 120R
(SCK/PCINT1) PB1	20	52	R20 22R RV18 120R
(SS/PCINT0) PB0	19	53	R34 22R
(A15) PC7	60	30	
(A14) PC6	59	31	
(A13) PC5	58	32	PC5
(A12) PC4	57	33	
(A11) PC3	56	34	E0-STEP
(A10) PC2	55	35	Z-STEP
(A9) PC1	54	36	Y-STEP
(A8) PC0	53	37	X-STEP
(T0) PD7	50	38	
(T1) PD6	49	83	XTRA_0
(XCK1) PD5	48	82	PD5
(ICP1) PD4	47	81	X_MAX
(TXD1/INT3) PD3	46	18	TX1
(RXD1/INT2) PD2	45	19	RX1
(SDA/INT1) PD1	44	20	
(SCL/INT0) PD0	43	21	SDA SCL
(CLKO/ICP3/INT7) PE7	9	80	TACH_1
(T3/INT6) PE6	8	79	TACH_0
(OC3C/INT5) PE5	7	pwm 3	HEAT-0
(OC3B/INT4) PE4	6	pwm 2	
(OC3A/AIN1) PE3	5	pwm 5	
(XCK0/AIN0) PE2	4	78	
(TXD0) PE1	3	1	TX0
(RXD0/PCIN8) PE0	2	0	RX0
(ADC7/TDI) PF7	90	A7	PF7
(ADC6/TDO) PF6	91	A6	PF6
(ADC5/TMS) PF5	92	A5	PF5
(ADC4/TCK) PF4	93	A4	
(ADC3) PF3	94	A3	Y_MAX
(ADC2) PF2	95	A2	THERM2
(ADC1) PF1	96	A1	THERM1
(ADC0) PF0	97	A0	THERM0
(OC0B) PG5	1	pwm 4	BED-HEAT
(TOSC1) PG4	29	70	PG4
(TOSC2) PG3	28	71	PG3
(ALE) PG2	70	39	Y_nCS
(RD) PG1	52	40	
(WR) PG0	51	41	X_nCS



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Atmega 32u2 USB

USB to Serial



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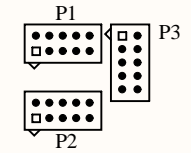


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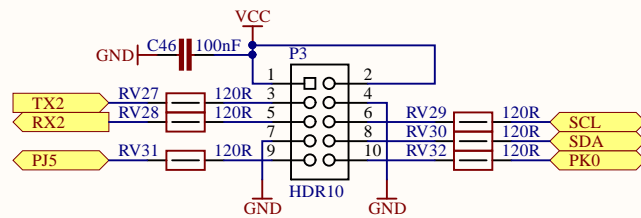
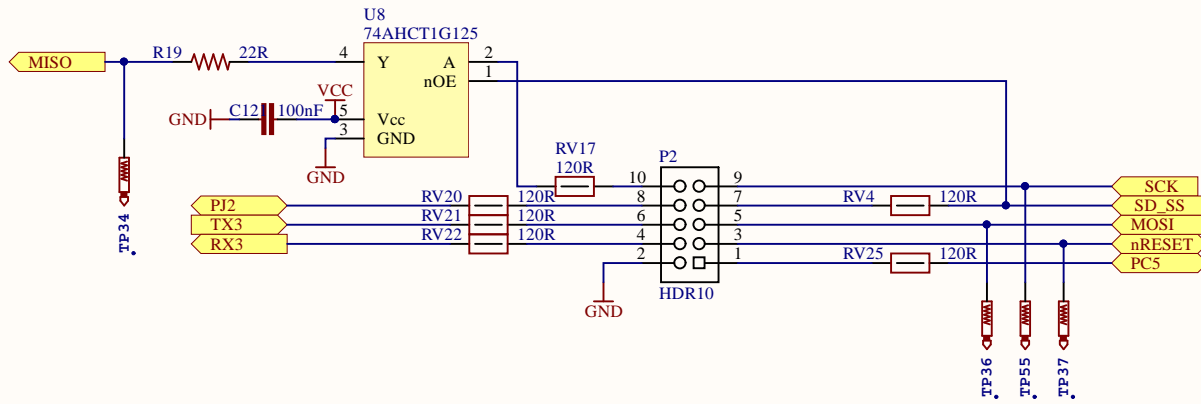
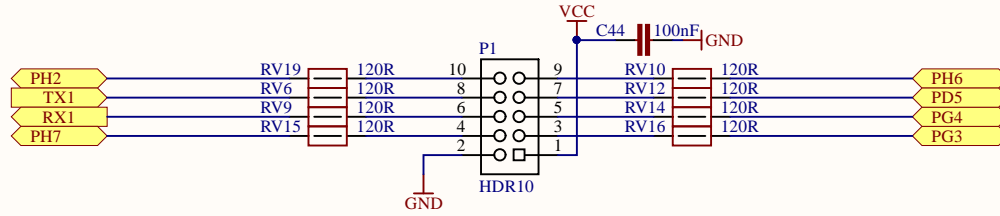
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Expansion Connectors

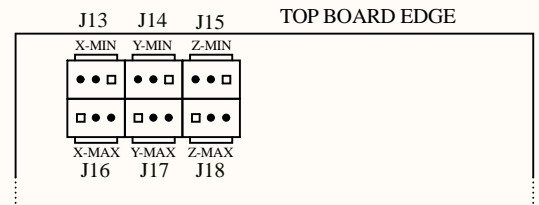
TOP BOARD EDGE



Connector Layout

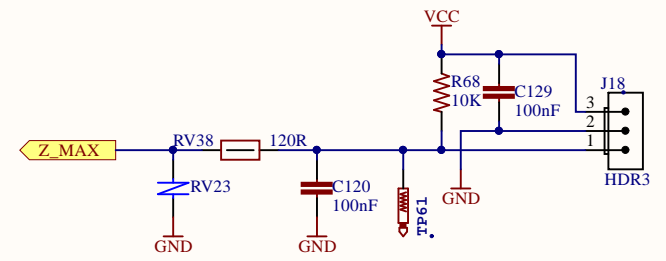
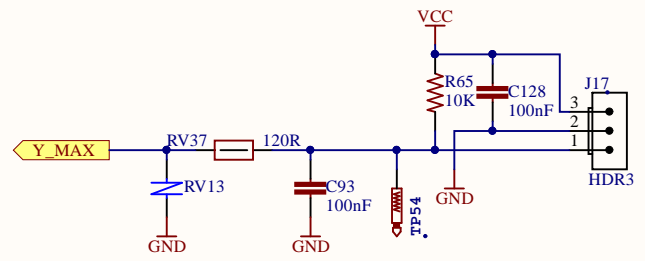
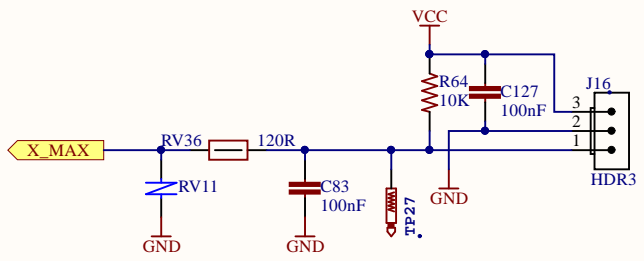
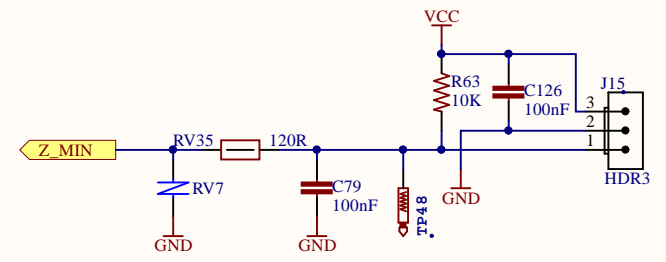
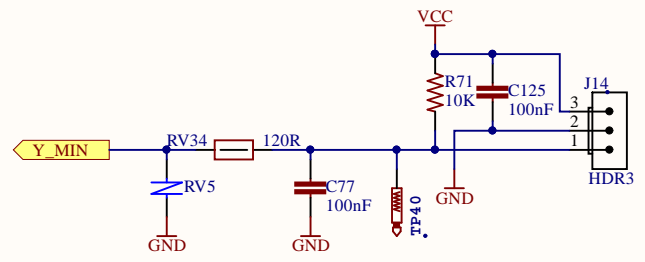
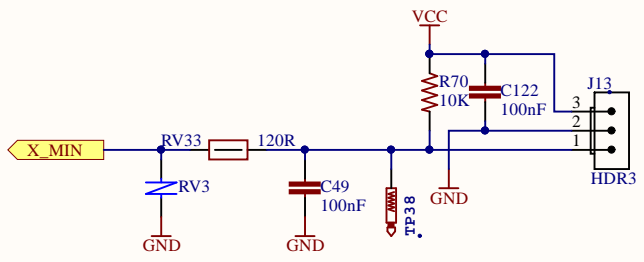


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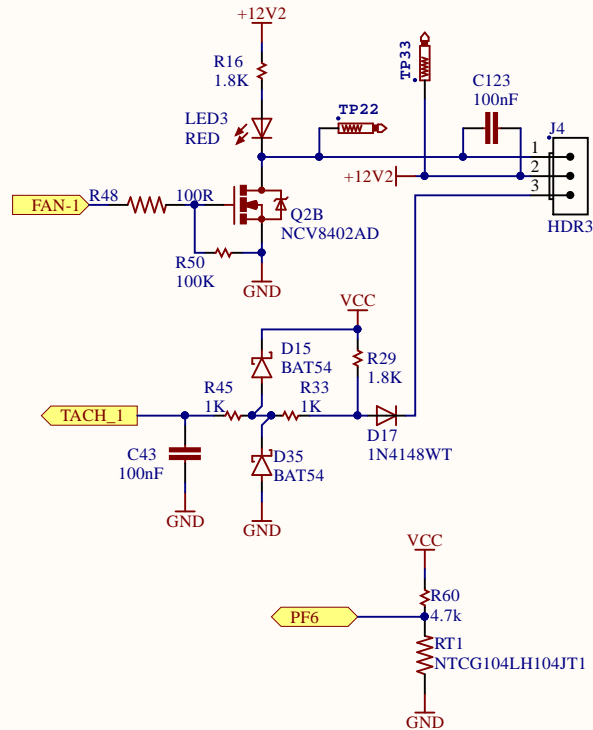
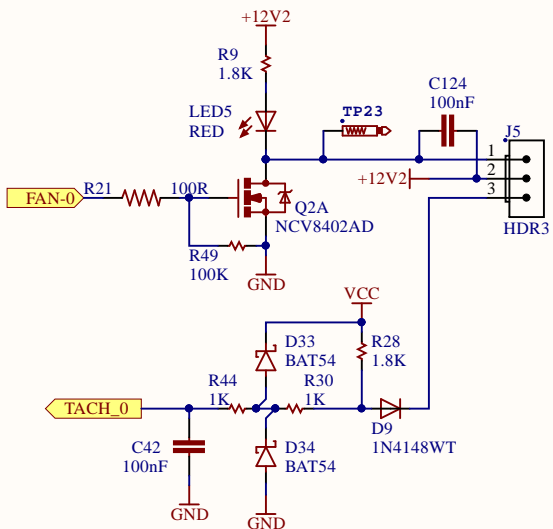
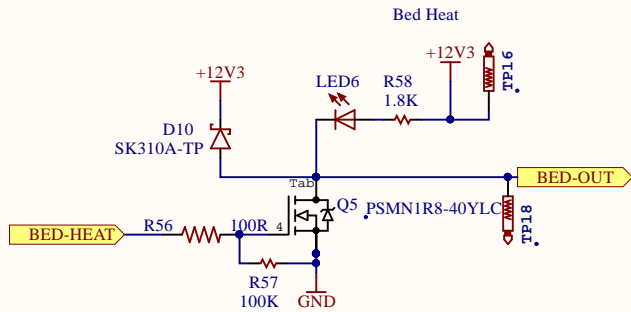
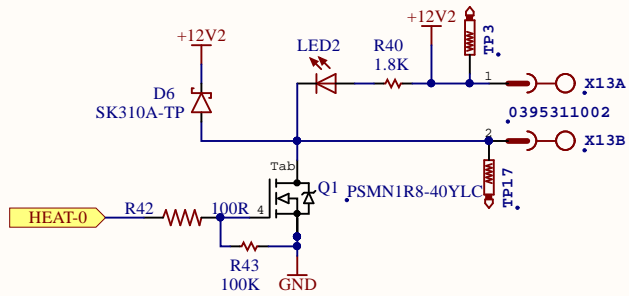
Connector Layout

End Stops

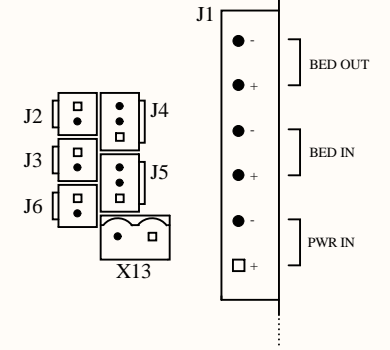


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Heater Outputs

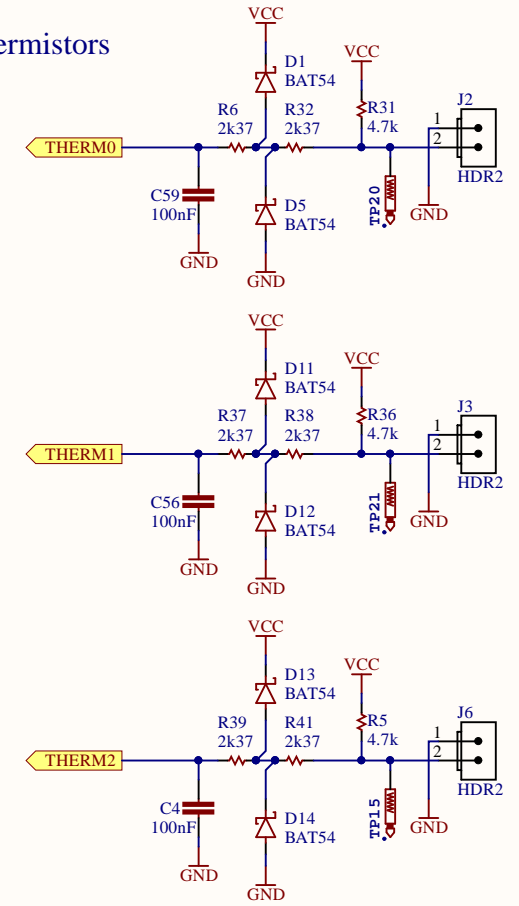


TOP BOARD EDGE



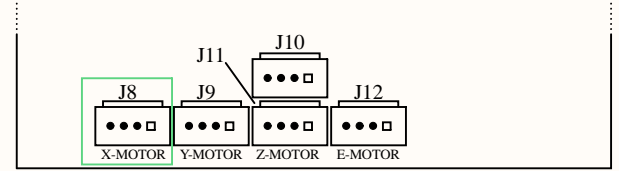
Connector
Layout

Thermistors

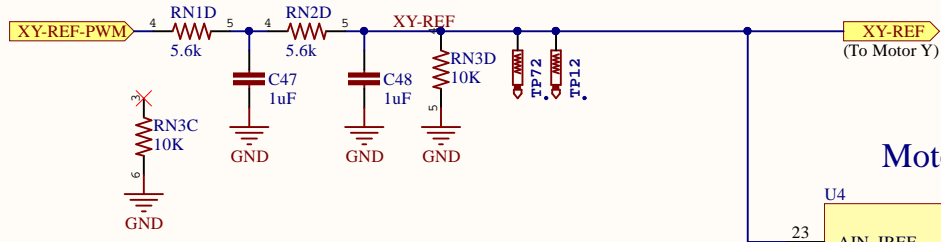


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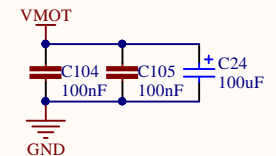
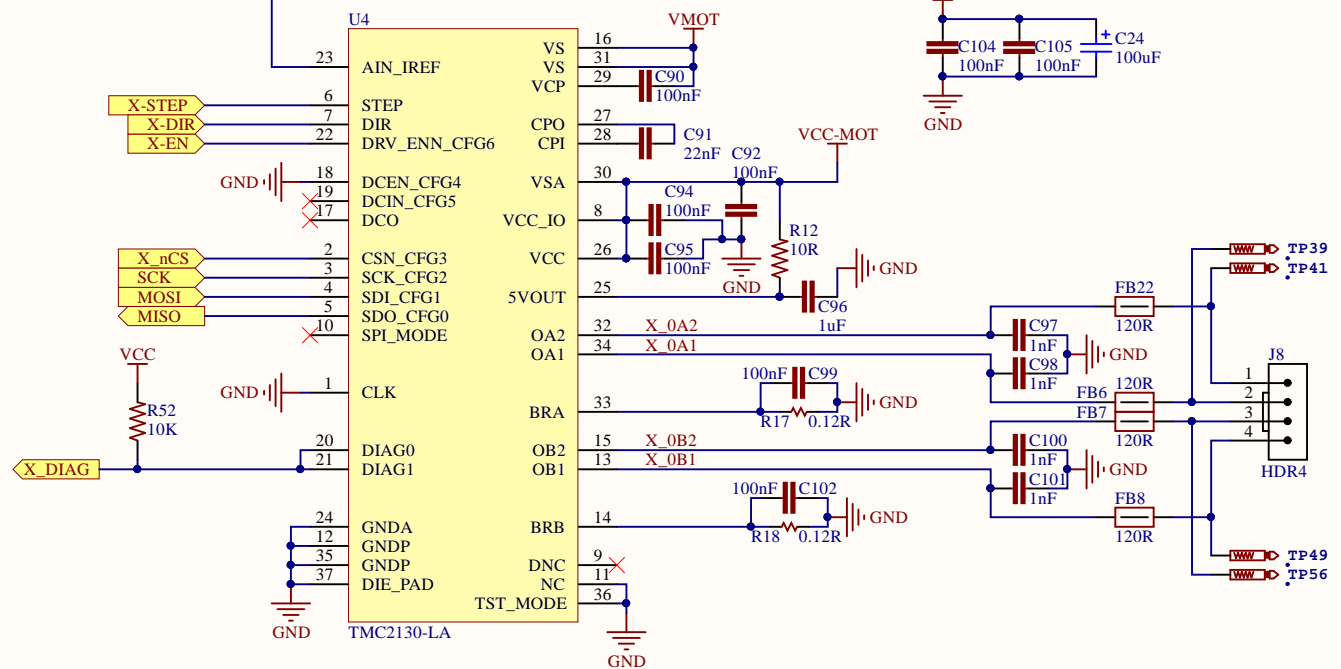
Connector Layout



BOTTOM BOARD EDGE



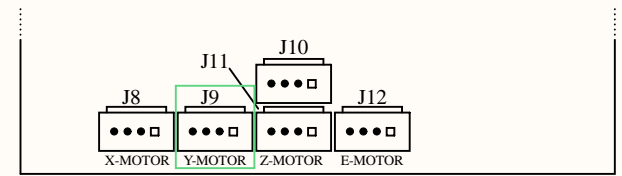
Motor X



Depricated Test Points	
X_OA1	TP75
X_OA2	TP73
X_OB1	TP1
X_OB2	TP74

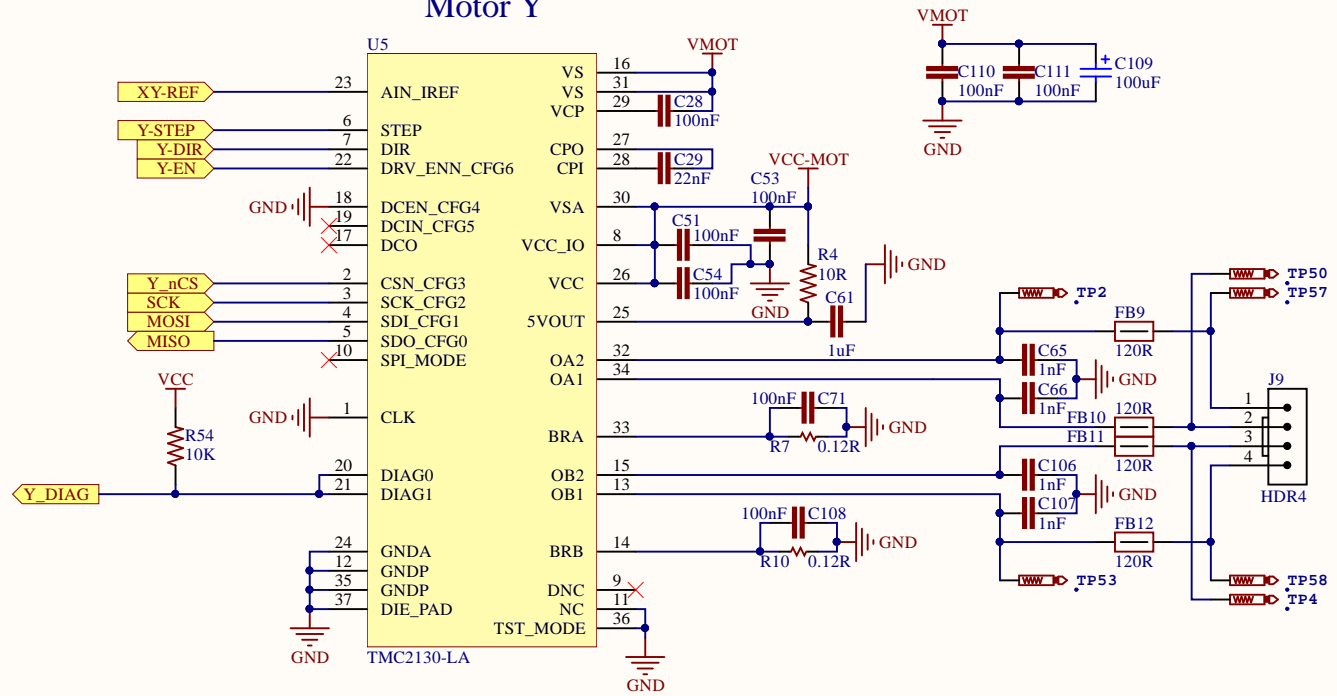
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Title: Motor-X	File: Motor-X.SchDoc
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Connector Layout

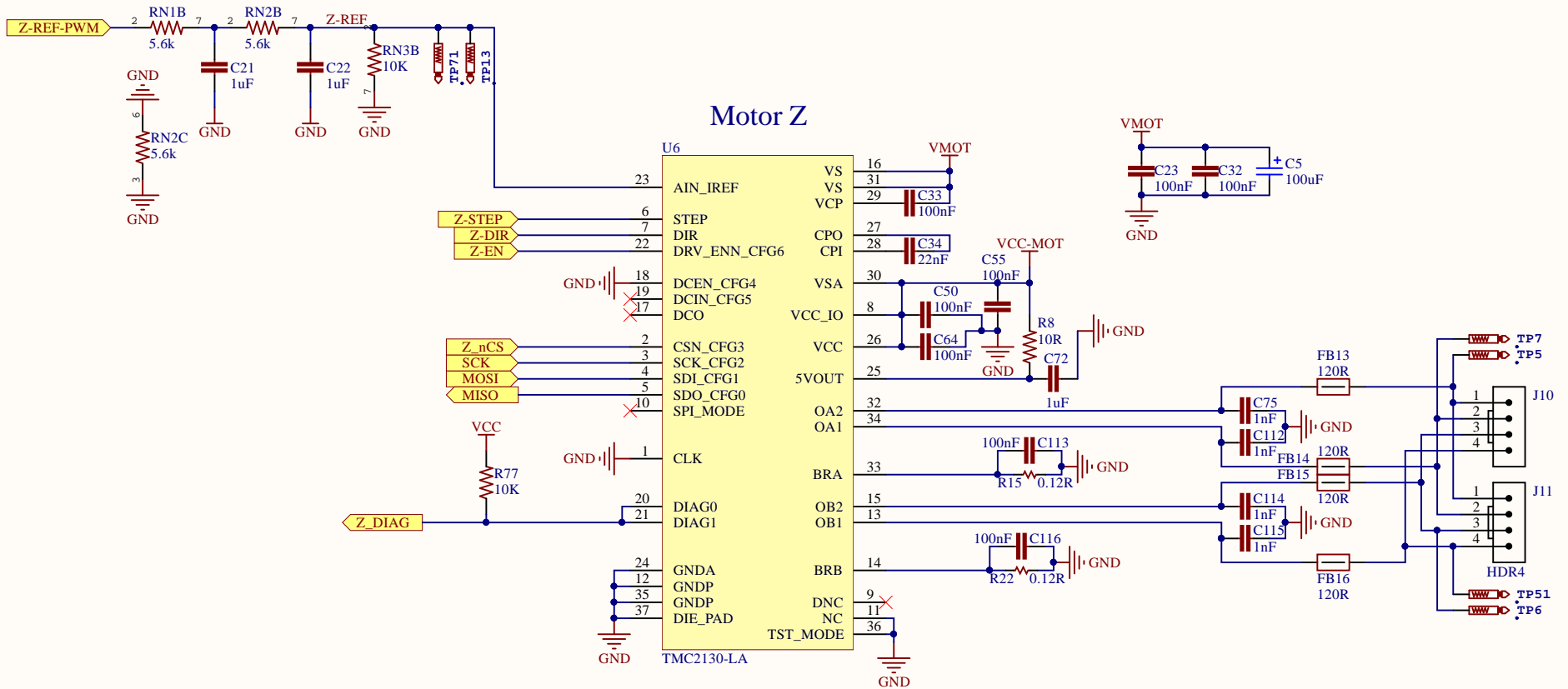
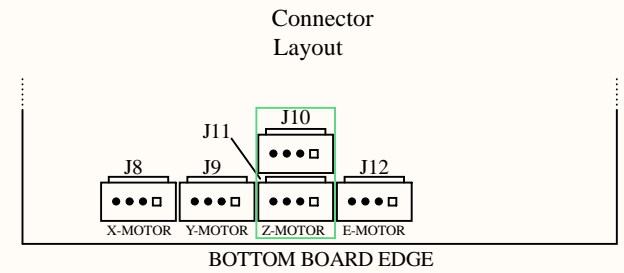


BOTTOM BOARD EDGE

Motor Y

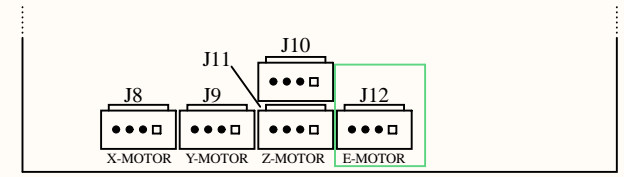


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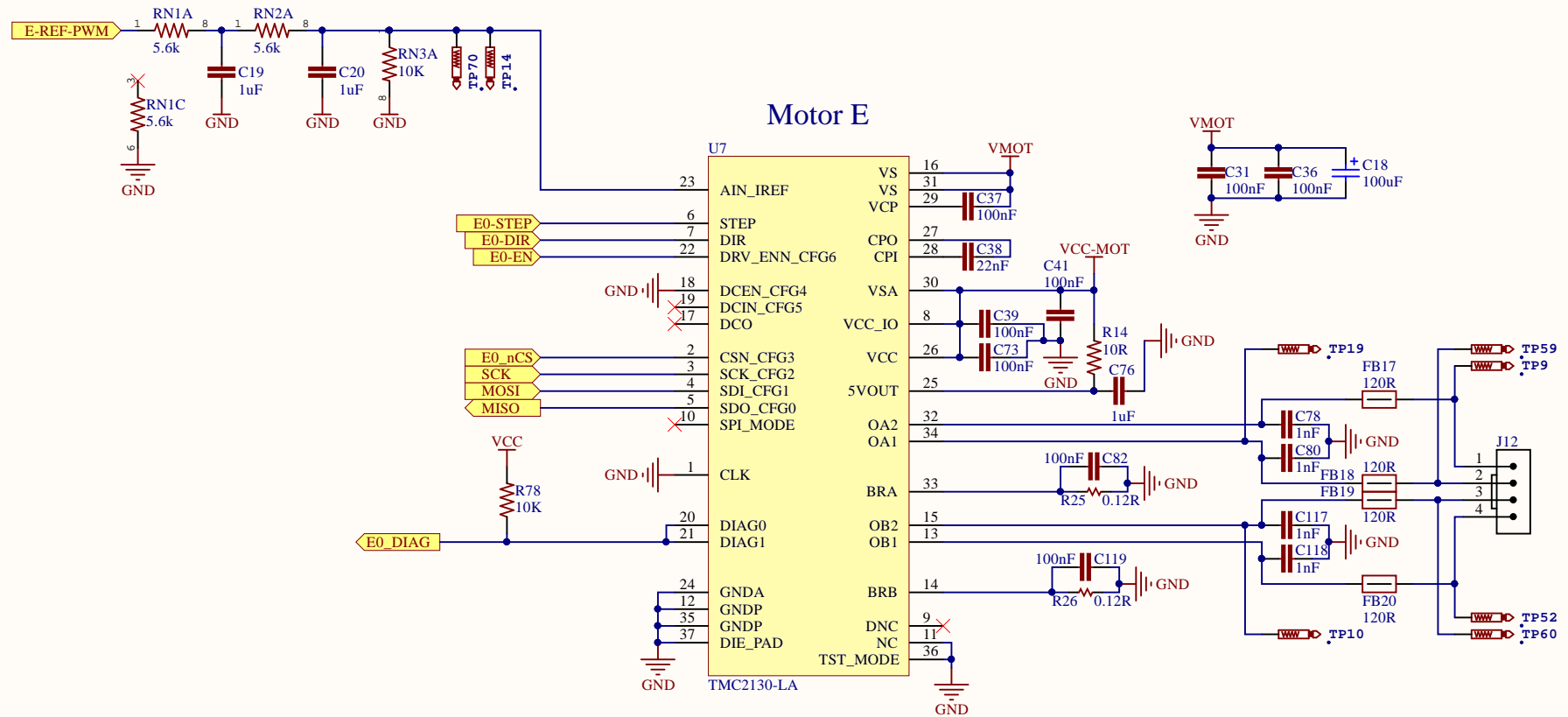


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Connector
Layout



BOTTOM BOARD EDGE



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